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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/010,737	12/07/2001	Atila Alvandpour	884.451US1	2666
21186	7590	09/22/2004	EXAMINER	
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.			TRAN, ANH Q	
P.O. BOX 2938			ART UNIT	PAPER NUMBER
MINNEAPOLIS, MN 55402			2819	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/010,737

Applicant(s)

ALVANDPOUR ET AL.

Examiner

Anh Q. Tran

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 19 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11, 17, 20 and 23-25 is/are rejected.
- 7) ☒ Claim(s) 12-16, 18-19, 21-22 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. In view of the appeal brief filed on 4/19/04, PROSECUTION IS HEREBY REOPENED. New ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 6-7, 9-11, and 23-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Nunogami (5,136,191).

Claim 1, Nunogami discloses a first logic unit (10, Fig. 1) connected to a first supply voltage (VDD1); a second logic unit (external system, col. 2, line 16) connected to a second supply voltage (VDD2, col. 2, line 12); and a voltage-level converter (2, Fig.

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1) connecting the first logic unit to the second logic unit, the voltage-level converter including at least one transistor (11) having a threshold voltage greater than or about equal to the difference between the second supply voltage and the first supply voltage (col. 2, lines 1-4) and the at least one transistor connected to the second supply voltage.

Claim 6, Nunogami discloses the voltage-level converter comprises an inverter (14).

Claim 7, Nunogami discloses the inverter comprises an n-type insulated-gate field-effect transistor (12) connected in series with the at least one transistor.

Claim 9, Nunogami discloses the voltage-level converter comprises a first inverter (14) coupled in series to a second inverter (17).

Claim 10, Nunogami discloses the first inverter includes the at least one transistor (12).

Claim 11, Nunogami discloses a first logic unit (10, Fig. 1) connected to a first supply voltage (VDD1); a second logic unit (external system, col. 2, line 16) connected to a second supply voltage (VDD2, col. 2, line 12); and a logic circuit (2) connecting the first logic unit to the second logic unit, the logic circuit including at least one transistor (11) having a threshold voltage greater than or about equal to the difference between the second supply voltage and the first supply voltage (col. 2, lines 1-4) and the at least one transistor connected to the second supply voltage (VDD2).

The apparatus described above is applicable to the method claims 23-25.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 2-5, 8, 17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nunogami (5,136,191) in of Aoki (5,610,544).

Nunogami discloses the claimed invention except for the first logic unit as a memory unit and the second logic unit as an arithmetic unit or a clock distribution circuit. It would have been an obvious matter of design choice to provide the first logic unit as a memory unit and the second logic unit as an arithmetic unit or a clock distribution circuit since it was known in the art that a voltage level converter is used for raising or lowering voltage level between any two logic unit having two different supply voltages which are teaches by Aoki (e.g., the first logic unit as a memory unit and the second logic unit as an arithmetic unit, CPU, or a clock distribution circuit, timer, col. 1, lines 15-55).

***Allowable Subject Matter***

5. Claims 12-16, 18-19, and 21-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

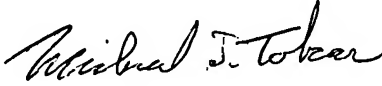
Reopening Prosecution and  
New Grounds of Rejection Approved

Anh Q. Tran  
Examiner  
Art Unit 2819

Michael Tokar  
Supervisory Primary Examiner  
Art Unit 2819



9/20/04

  
Michael Tokar  
Supervisory Patent Examiner  
Technology Center 2800